AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A decoder circuit used in a flash memory device comprising:

a global row decoder for outputting a global word line signal, said global row decoder consisted of a first decoding means selected according to a row address signal and a second decoding means to which an output signal of said first decoding means and an erasure signal are input; and

a local row decoder for selecting a word line by a global word line signal outputted from said global row decoder.

2. (Original) The decoder circuit of claim 1, wherein said first and second decoding means are consisted of NAND gates.

3. (Currently Amended) The decoder circuit of claim 1, wherein said local row decoder is consisted of:

a first switching element for transferring a column sector address to a node according to said global word line signal;

a second switching element for transferring a first signal to said node according to said global word line signal;

a third switching element connected, in parallel, with said ~~first~~ second switching element, said third switching element operated by potential of a word line;

a fourth switching element for transferring ~~a~~ said first signal to said word line according to potential of said node; and

a fifth switching element for transferring a second signal to said word line according to potential of said node.

4. (Currently Amended) The decoder circuit of claim 3, wherein said second, third and fourth switching elements are consisted of PMOS transistor, respectively, and each of said first and fifth switching elements ~~are~~ is consisted of ~~a~~ an NMOS transistor~~, respectively~~.

5. (Currently Amended) A decoder circuit used in a flash memory device, comprising:

a global row decoder for outputting a global word line signal, wherein said global row decoder comprises:

a first transistor for transferring a first ~~volatage~~ voltage to a node according to a first signal;

a second transistor for transferring a ground voltage to said node according to said first signal;

a third transistor for transferring a second voltage to a global word line according to potential of said node; and

a fourth transistor for transferring said first voltage to said global word line according to potential of said node;

a local row decoder for selecting a word line in response to said global word line signal of said global row decoder, wherein said local row decoder comprises:

a fifth transistor for transferring said global word line signal to said word line in response to a second signal;

a sixth transistor for transferring said global word line signal to said word line according to a third signal; and

a seventh transistor for transferring a ground voltage to said word line in response to said second signal.

6. (Canceled)

7. (Currently Amended) The decoder circuit of claim 6, wherein said first and third transistors are consisted of PMOS transistor, and each of said second and fifth transistors ~~are~~ is consisted of an NMOS transistor.

8. (Canceled)

9. (Currently Amended) The decoder circuit of claim 8, wherein said fifth transistor is consisted of a PMOS transistor, and each of said sixth and seventh transistors ~~are~~ is consisted of an NMOS

transistor.

a fourth transistor for transferring said first voltage to said global word line according to potential of said node;

a local row decoder for selecting a word line in response to said global word line signal of said global row decoder, wherein said local row decoder comprises:

a fifth transistor for transferring said global word line signal to said word line in response to a second signal;

a sixth transistor for transferring said global word line signal to said word line according to a third signal; and

a seventh transistor for transferring a ground voltage to said word line in response to said second signal.

6. (Canceled)

TP 7. (Currently Amended) The decoder circuit of claim 5, wherein said first and third transistors are consisted of PMOS transistor, and each of said second and fifth transistors ~~are~~ is consisted of an NMOS transistor.

8. (Canceled)

TP 9. (Currently Amended) The decoder circuit of claim 7, wherein said fifth transistor is consisted of a PMOS transistor, and each of said sixth and seventh transistors ~~are~~ is consisted of an NMOS